CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A SiGe heterojunction bipolar transistor structure comprising:

a patterned SiGe base structure which includes at least a SiGe layer present atop a substrate and a patterned insulator present on a portion of said SiGe layer having an opening that exposes a portion of said SiGe layer; and

an emitter layer formed atop said SiGe base structure including in said opening, said emitter layer is a bilayer of in-situ P-doped a:Si and in-situ P-doped polysilicon.

2. The SiGe heterojunction bipolar transistor structure of Claim 1 wherein said SiGe layer comprises a single crystal SiGe base region which is sandwiched between polycrystalline SiGe regions.

3. The SiGe heterojunction bipolar transistor structure of Claim 1 wherein said SiGe layer is present atop a semiconductor substrate, said semiconductor substrate including a collector region present atop a subcollector region.

4. The SiGe heterojunction bipolar transistor structure of Claim 3 wherein said semiconductor substrate further includes isolation regions which define outer boundaries of said bipolar transistor.

5. The SiGe heterojunction bipolar transistor structure of Claim 1 further comprising an oxide layer present atop said exposed portion of said SiGe layer.

6. The SiGe heterojunction bipolar transistor structure of Claim 1 wherein said in-situ doped-P a:Si is a recrystallized in-situ doped-P layer.

7. The SiGe heterojunction bipolar transistor structure of Claim 1 wherein said patterned insulator is comprised of SiO_2, Si oxynitride or a combination thereof.

8. The SiGe heterojunction bipolar transistor structure of Claim 1 further comprising an outdiffused P-dopant region present in said exposed portion of said SiGe layer beneath said opening.

9. The SiGe heterojunction bipolar transistor structure of Claim 1 wherein said SiGe layer is doped with boron.

10. A method of fabricating a SiGe heterojunction bipolar transistor comprising

forming an emitter layer atop a patterned SiGe base structure, wherein said emitter layer is a bilayer of in-situ P-doped a:Si and in-situ P-doped polysilicon.

11. The method of Claim 10 further comprising thermal growing an oxide layer atop a portion of said patterned SiGe base structure prior to forming said emitter layer.

12. The method of Claim 11 wherein said oxide layer is formed utilizing a rapid thermal oxidation process which is performed in an oxygen-containing atmosphere at a temperature of about 600°C or greater.

13. The method of Claim 11 wherein said oxide layer is formed atop exposed portions of a single crystal SiGe region present in said SiGe layer.

14. The method of Claim 10 wherein said bilayer is formed using a rapid thermal chemical vapor deposition process wherein the temperature of emitter deposition is about 600°C or greater for a time period of about 2 minutes or less.

15. The method of Claim 10 further comprising subjecting said in-situ P-doped a:Si layer to a recrystallizing annealing step prior to forming said in-situ P-doped polysilicon.

16. The method of Claim 15 wherein said recrystallizing annealing is carried out at a temperature of about 630°C or greater for a time period of about 30 minutes or less.

17. The method of Claim 10 further comprising subjecting said emitter bilayer to an activation annealing which is capable of driving- P-dopant into a portion of a single crystal SiGe region of the structure.

18. The method of Claim 17 wherein said activation annealing is performed at a temperature of about 950°C or less.

19. The method of Claim 10 wherein said SiGe base structure includes at least a SiGe layer present atop a substrate and a patterned insulator present on a portion of said SiGe layer having an opening that exposes a portion of said SiGe layer.

20. The method of Claim 19 wherein said SiGe layer includes a single crystal SiGe region present beneath said opening and polycrystalline SiGe regions abutting said single crystal SiGe region.